REMARKS

Claims 1-22 are pending in this application. By this amendment, claims 1 and 14 are amended. Reconsideration and allowance of the application is respectfully requested.

Amendment After Final Rejection

Entry of the Amendment is request under 37 C.F.R. § 1.116 because the Amendment: a) places the application in condition for allowance for the reasons discussed herein; b) does not present any additional claims without canceling the corresponding number of final rejected claims; and c) places the application in better form for appeal, if an appeal is necessary. Entry of the Amendment is thus respectfully requested.

Allowable Subject Matter

Applicants appreciate that claims 1-13 and 21 are allowed; and claims 2-7 and 16-20 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the features of a base claim and any intervening claims. However, it is respectfully submitted that claims 1, 8 and 14-15 are also allowable in view of the foregoing amendments and the following remarks.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 8, 14, and 15 are rejected under 35 U.S.C. § 102(b) as being anticipated by Takaya, U.S. Patent 5,783,967. This rejection is respectfully traversed.

Independent claim 1 recites, *inter alia*, "the control signal controls a duration of the time delay applied to the first clock signal by the delay circuit, the control signal is increased or decreased in response to a logic signal", as recited in claim 1.

Takaya discloses in Fig. 2 a multiplier circuit having a first and second voltage control delay circuits 22, 23, a phase comparator 24 for comparing the phase of the input signal with the phase of an output signal of the second voltage control delay circuit 23, a loop filter circuit 25 responsive to the output signal of the phase comparator 24 for producing a control signal for controlling the first and second voltage control delay circuits 22, 23 to automatically correct a delay thereof such that an input signal passing through the first and second voltage control delay circuits 23, 24 is delayed in phase by 180°, and an exclusive OR circuit 26 receptive of the input signal and the output signal of the first voltage control delay circuit 22 for outputting a double frequency output signal having a duty ratio of 50% (col. 2, lines 26-35 and col. 3, lines 43-49). However, Applicants' submit that the control signal of Takaya fails to disclose or even mention increasing or decreasing in response to a logic signal.

As an example embodiment of the present invention, Fig. 3 illustrates a first period, a second period, and a third period based on changes in the timing of the first clock signal CLK 1 and the delayed clock signal CLKD. In the first period, during which the first voltage V1 increases, the first clock signal CLK 1 may be high, and the delayed clock signal CLKD may be low. In the second period during which the first voltage V1 decreases, both the first clock signal CLK 1 and the delayed clock signal CLKD may be high. In the third period, during which the first voltage V1 and the second voltage V2 may be reset to the same level, the first clock signal CLK 1 may be low and the delay clock signal CLKD may be high.

Takaya fails to disclose or suggest that the control signal is increased or decreased in response to a logic signal, as described above or as recited in claim 1.

Accordingly, for at least these reasons, claim 1 and those claims dependent thereon are allowable over the applied art.

Applicants further submit for the similar reasons as those stated above with regard to claim 1, that claim 14 and those claims dependent thereon are also allowable over the applied art. Withdrawal of the rejection is also respectively requested.

Accordingly, Applicants respectfully submit that for at least the reasons stated above, all currently pending claims 1-21 are now in condition for allowance. Withdrawal of any outstanding rejections and allowance of these claims are respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-22 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano, Reg. No. 35,094 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
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